(VREF1). One of more latches 76 store the digital bits and can be enabled to transmit the bits to the bus 54.

Please rewrite the paragraph at page 20, lines 4-12 as follows:

The amplified differential analog signal then is converted to a corresponding digital signal by the ADC 74. In the implementation of FIG. 4, the ADC 74 includes a comparator 92 and a binary-scaled network of capacitors C11-C18. Details of an exemplary comparator circuit 92 are illustrated in FIG. 8. The comparator 92 includes positive and negative terminals and an output. A "strobe" signal enables the comparator 92 to provide an output signal based on the signals at its positive and negative terminals.

Please rewrite paragraph at page 25, line 16 - page 26, line 8 as follows:

Returning now to FIG. 4, the circuit 52 also includes a calibration network 72 to provide corrections for the analog-to-digital conversion based, for example, on the offset of the comparator 92. The calibration network 72 also includes a network of small capacitors C19-C26 whose upper plates are electrically connected to the upper plates of capacitors C11, C12, C18 in the ADC binary-scaled network. Each capacitor C19-C26 has a respective latch and logic associated wit. For example, the capacitors C19, C24 have respective latches 102 and logic 100 associated with them and can be connected to either zero volts or a reference voltage VREF2. Similarly, the capacitor C25 has a latch 106 controlled by logic 104 associated with it and can be connected to either zero voltage or the reference voltage VREF2. The capacitor C26 has a latch 110 and controlled by logic 108 associated with it and can be connected to either zero volts or the reference voltage VREF3.